FIRST EDITION

Hardware Engineer Interview Questions

141 board-level electrical engineering questions with model answers on power, signal integrity, analog, PCB and embedded design — from a board designer with 30 years at the bench

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Hardware Engineer Interview Questions: 141 Board-Level Electrical Engineering Questions with Model Answers on Power, Signal Integrity, Analog, PCB and Embedded Design
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Editorial note. This book grew out of years of hardware interviews seen up close. The author has taken many interviews himself, has mentored and worked alongside many junior engineers and heard how their interviews went, and still helps new graduates and master's and PhD candidates prepare for theirs. The questions are the problems that kept coming up, gathered naturally over that time and rewritten as representative engineering problems. Questions, scenarios and engineering judgement come from the author's own notes and experience; the text was drafted with AI assistance and reviewed by the author. No company names, interviewer material, interview guides or take-home assignments are reproduced. Scenarios are generic, and every number in a question is an illustrative assumption, not data from any product or company. The questions are not a ranked list of what any company asks. The "Track" line says which reading path a question belongs to.

Answers reflect the author's engineering judgement. Numbers are typical values for estimation, not specifications — always check the datasheet and the standard.

How to use this book

Every question sits on a **right-hand page**. Its answer is on the **back of the same sheet**. Print double-sided, read the question, answer it out loud, then turn the page.

Each question page shows:

- **Track** — the reading path: General board · Power · SI & high-speed · Embedded & wearables · Senior system. Read one track at a time if you are short on time.
- **Level** — ● screening · ●● onsite technical · ●●● onsite design / senior.
- **What they are really testing** — the skill behind the question.

Each answer page shows:

- **Say this first** — the 2–3 sentence answer to give in the first 30 seconds.
- **Then explain** — the working, drawn the way you would draw it on a whiteboard.
- **Numbers to quote** — the values that make an interviewer trust you.
- **Follow-ups** — where a good interviewer goes next.
- **Going deeper** — the web address of the question's own page at hwinterview.com, with a longer explanation, diagrams and reader questions.

How Silicon Valley hardware interviews work

The loop. A recruiter call, then a 45–60 min technical screen with an engineer (your resume plus fundamentals), then an onsite or virtual loop of 4–6 interviews, 45 min each:

Interview	What happens
Technical ×2	Fundamentals, theory and applied: op-amps, power, SI, interfaces. Deep follow-ups.
Design ×1	An open problem ("design a power system for…"). No single right answer.
Hands-on / debug (some companies)	A broken circuit and a scope, or a schematic to review.
Behavioral ×1	Conflict, failure, ownership — told as stories.
Partnership / cross-functional ×1	How you work with ME, firmware, product, suppliers.

Most loops end with 5 minutes for your questions. Virtual loops use a shared whiteboard tool; practice drawing a buck converter and an op-amp with a mouse before the day.

What they grade, in every interview

1. **Clarifying questions.** The best answers start with questions: voltage, current, bandwidth, load profile, cost, size.
2. **Fundamentals over memory.** Derive from first principles (KCL, V = L·di/dt, the op-amp rules), not recited formulas.
3. **Numbers.** Put an order-of-magnitude number on everything. "About 1 mΩ" beats "very low".
4. **Trade-offs.** Every design choice costs something. Say what it costs.
5. **Debug thinking.** Hypothesis → measurement → narrow down. Never "replace parts until it works".
6. **Ownership of your resume.** Draw the block diagram of every project you list, and say why you chose each major part.

A 6-step answer frame for design questions

1. Restate the problem and ask 3–5 clarifying questions.
2. State your assumptions out loud and write them on the board.
3. Draw the block diagram first, then the detail.
4. Put numbers on it (power budget, ripple, bandwidth, timing).
5. Name the risks and the trade-offs.
6. Say how you would verify it (simulation, bench test, margin).

Behavioral answers use a story frame — Situation, Action, Impact, Learning (or STAR). Prepare 6 stories that you can bend to fit any question: a hard technical bug, a disagreement, a failure, leading without authority, a schedule crunch, and mentoring someone.

Contents

1	Passives & Components	10	9
2	Analog & Op-Amps	16	31
3	Filters, Sampling & Data Converters	7	65
4	Power Conversion	20	81
5	Power Integrity & Protection	5	123
6	Signal Integrity & Transmission Lines	16	135
7	High-Speed Interfaces & Memory	14	169
8	Low-Speed Interfaces & Embedded Hardware	12	199
9	EMC, ESD & Grounding	8	225
10	PCB Layout, Stack-up & Manufacturing	8	243
11	Measurement, Debug & Failure Analysis	9	261
12	System Design (Open-Ended)	10	281
13	Behavioral & Your Own Story	6	303
	Appendix A — Numbers to carry · B — Index		317

CHAPTER 1

Passives & Components

Every design question eventually becomes a part-selection question. Interviewers use components to see whether you know how real parts differ from ideal ones — derating, parasitics, and failure modes.

10 questions

In this chapter

PC-01	Choosing a capacitor type	●
PC-02	MLCC field failure at cold	●●
PC-03	Ferrite bead selection	●●
PC-04	Common-mode choke vs ferrite bead	●●
PC-05	Schottky reverse recovery	●
PC-06	Zener in a divider	●
PC-07	MOSFET loss trade-off	●●
PC-08	Inductor soft vs hard saturation	●●
PC-09	MLCC acoustic noise	●●
PC-10	Two-capacitor paradox	●●

CHOOSING A CAPACITOR TYPE

You need bulk and decoupling capacitance on a 5 V rail. Compare ceramic (MLCC), tantalum, polymer and aluminum electrolytic capacitors. Where would you use each?

Track	General board
Level	●
Really testing	Whether you know real capacitors lose capacitance with DC bias and temperature, and how ESR shapes the choice.

Your answer — say it out loud, then sketch it:

Answer on the back →

PC-01 Choosing a capacitor type

> **Say this first:** MLCCs for high-frequency decoupling — small, low ESR/ESL, no wear-out — but they lose most of their capacitance under DC bias and at temperature extremes. Polymer/tantalum for dense bulk at higher bias. Aluminum electrolytic for cheap, large bulk where size and lifetime allow, and where some ESR helps damp the input.

Then explain

- **MLCC (X5R/X7R):** a 10 µF 0603 X5R at 5 V may give only 3–4 µF. Read the DC-bias curve, not the label. Piezoelectric — can "sing" (audible noise) with ripple in the kHz range.
- **Tantalum (MnO_2):** best µF per volume, stable with bias; must be derated ~50% in voltage; can fail short and burn under surge.
- **Polymer (tantalum or aluminum):** low ESR, self-healing, benign failure, only ~10–20% voltage derating needed.
- **Aluminum electrolytic:** large C cheaply, high ESR, dries out — life halves for every 10 °C hotter it runs.

Numbers to quote: MLCC loses 50–80% of its C at rated voltage in small cases · tantalum derate to ~50% V · e-cap life doubles for every 10 °C cooler.

Follow-ups: "Why put a lossy cap at a wall-adapter input?" — cable inductance + pure MLCC = high-Q LC tank; plug-in rings to 2× Vin. ESR of a polymer/electrolytic damps it.

MLCC FIELD FAILURE AT COLD

A product with a 100 µF ceramic output capacitor bank glitches in the field at −40 °C. What do you suspect?

Track	General board
Level	●●
Really testing	Temperature and DC-bias derating stacking up; loop stability that depends on Cout.

Your answer — say it out loud, then sketch it:

Answer on the back →

PC-02 MLCC field failure at cold

> **Say this first:** The effective capacitance collapsed. Temperature coefficient plus DC bias can turn "100 µF" into ~40 µF or less, which raises ripple, slows transient response, and can move the regulator's loop crossover until it rings or trips UVLO.

Then explain

- X5R/X7R allow ±15% over temperature; Y5V allows +22/−82% and Z5U +22/−56%.
- DC bias derating stacks on top of that: a 3–5 V bias on a small-case MLCC can remove another 40–60%.
- A converter compensated for 100 µF now has a higher LC resonance and less phase margin → load steps overshoot or ring.

What to do: characterize C at −40 °C *and* at Vout; use larger cases or higher-voltage-rated parts; add a polymer cap; re-check phase margin at the cold corner.

Follow-ups: "How would you prove it?" — Bode plot (loop injection) in a thermal chamber at −40 °C, compared with room temperature.

FERRITE BEAD SELECTION

How do you choose a ferrite bead for a power rail filter? What goes wrong if you pick by the rated current?

Track	General board
Level	●●
Really testing	Knowing that bead impedance collapses with DC bias and that beads can create resonances.

Your answer — say it out loud, then sketch it:

Answer on the back →

PC-03 Ferrite bead selection

> **Say this first:** Choose by the impedance curve at the noise frequency *at your DC current*, not the 100 MHz headline number. DC bias saturates the ferrite — at half the rated current impedance can drop by 90%. Rated current is a thermal limit, not an operating point; I run beads at ~20–30% of rating.

Then explain

- Bead = inductor + resistive loss (good — it dissipates noise) + parasitic C (it stops working above SRF).
- Bead + downstream decoupling cap forms an LC low-pass — it can **resonate and amplify** noise near f = 1/(2π√(LC)) if the Q is high. Add damping (a series R or a lossy cap).
- DC resistance causes IR drop — check it on a low-voltage rail.

Numbers to quote: 100 Ω @ 100 MHz bead can fall to ~10 Ω at 50% rated current.

Follow-ups: "Bead or common-mode choke on USB?" → see PC-04.